Amendments of the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the above-identified patent application:

Listing of Claims

1-54. (canceled)

55. (newly presented) A semiconductor comprising:

a substrate having a downwardly extending cavity formed therein;

a first spiral conductor formed in the cavity, said first spiral conductor being fabricated substantially in a first horizontal plane within the cavity; and

a second spiral conductor formed in the cavity, said second spiral conductor being fabricated substantially in a second horizontal plane within the cavity and above the first plane, wherein the first and second spiral conductors are positioned to be inductively coupled during operation.

56. (newly presented) The semiconductor of claim 55 wherein the first and second spiral conductors have an inductive coupling coefficient greater than about 0.8.

57. (newly presented) The semiconductor of claim 55 wherein:

each of said inductors has a center; and

said centers are substantially aligned along an axis.

58. (newly presented) The semiconductor of claim 57 wherein:

said first inductor has a first number of turns; and

said second inductor has a second number of turns.

59. (newly presented) The semiconductor of claim 58 wherein said first and second numbers are equal.

60. (newly presented) The semiconductor of claim 59 wherein:

said semiconductor has a major surface defining a plane; and

said cavity is formed in said major surface.

61. (newly presented) The semiconductor of claim 60 wherein said cavity comprises:

a bottom surface substantially parallel to said plane; and

a side wall substantially perpendicular to said plane.

62. (newly presented) The semiconductor of claim 60 wherein said cavity comprises:

a bottom surface substantially parallel to said plane; and

a side wall at an oblique angle relative to said plane.

63. (newly presented) The semiconductor of claim 62 wherein said side wall is at an angle of about 54.74° relative to said plane.

64. (newly presented) The semiconductor of claim 58 wherein:

said semiconductor has a major surface defining a plane; and

said cavity is formed in said major surface.

65. (newly presented) The semiconductor of claim 64 wherein said cavity comprises:

a bottom surface substantially parallel to said plane; and

a side wall substantially perpendicular to said plane.

66. (newly presented) The semiconductor of claim 64 wherein said cavity comprises:

a bottom surface substantially parallel to said plane; and

a side wall at an oblique angle relative to said plane.

67. (newly presented) The semiconductor of claim 66 wherein said side wall is at an angle of about 54.74° relative to said plane.

68. (newly presented) The semiconductor of claim 57 wherein:

said semiconductor has a major surface defining a plane; and

said cavity is formed in said major surface.

69. (newly presented) The semiconductor of claim 68 wherein said cavity comprises:

a bottom surface substantially parallel to said plane; and

a side wall substantially perpendicular to said plane.

70. (newly presented) The semiconductor of claim 68 wherein said cavity comprises:

a bottom surface substantially parallel to said plane; and

a side wall at an oblique angle relative to said plane.

71. (newly presented) The semiconductor of claim 70 wherein said side wall is at an angle of about 54.74° relative to said plane.

72. (newly presented) A semiconductor signal splitter comprising:

a first spiral conductor fabricated substantially in a first horizontal plane;

a second spiral conductor fabricated substantially in a second horizontal plane above the first plane; and

a third spiral conductor fabricated substantially in a third horizontal plane above the second plane, wherein the first, second and third spiral conductors are axially aligned, such that the first and second spiral conductors are positioned to be inductively coupled during operation, and the second and third spiral conductors are positioned to be inductively coupled during operation.

73. (newly presented) The semiconductor signal splitter of claim 72 wherein:

the first spiral conductor comprises n_1 turns;

the second spiral conductor comprises n_2 turns;

the third spiral conductor comprises n_3 turns;

a time-varying current waveform with amplitude (I) applied to the second spiral conductor produces an time-varying voltage output waveform from the first spiral conductor having an amplitude porportional to $(n_1/n_2)I$, and a time-varying voltage output waveform from the third spiral conductor having an amplitude proportional to $(n_3/n_2)I$.

74. (newly presented) The semiconductor signal splitter of claim 72 wherein the first, second and third spiral conductors are located within a semiconductor substrate well.

75. (newly presented) The semiconductor signal splitter of claim 74 wherein:

said spiral conductors are fabricated in a semiconductor substrate having a major surface defining a plane; and

said well is formed in said major surface.

76. (newly presented) The semiconductor signal splitter of claim 75 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall substantially perpendicular to said plane.

77. (newly presented) The semiconductor signal splitter of claim 75 wherein said well comprises:

a bottom surface substantially parallel to said plane; and

a side wall at an oblique angle relative to said plane.

78. (newly presented) The semiconductor signal splitter of claim 77 wherein said side wall is at an angle of about 54.74° relative to said plane.